

Fig.1

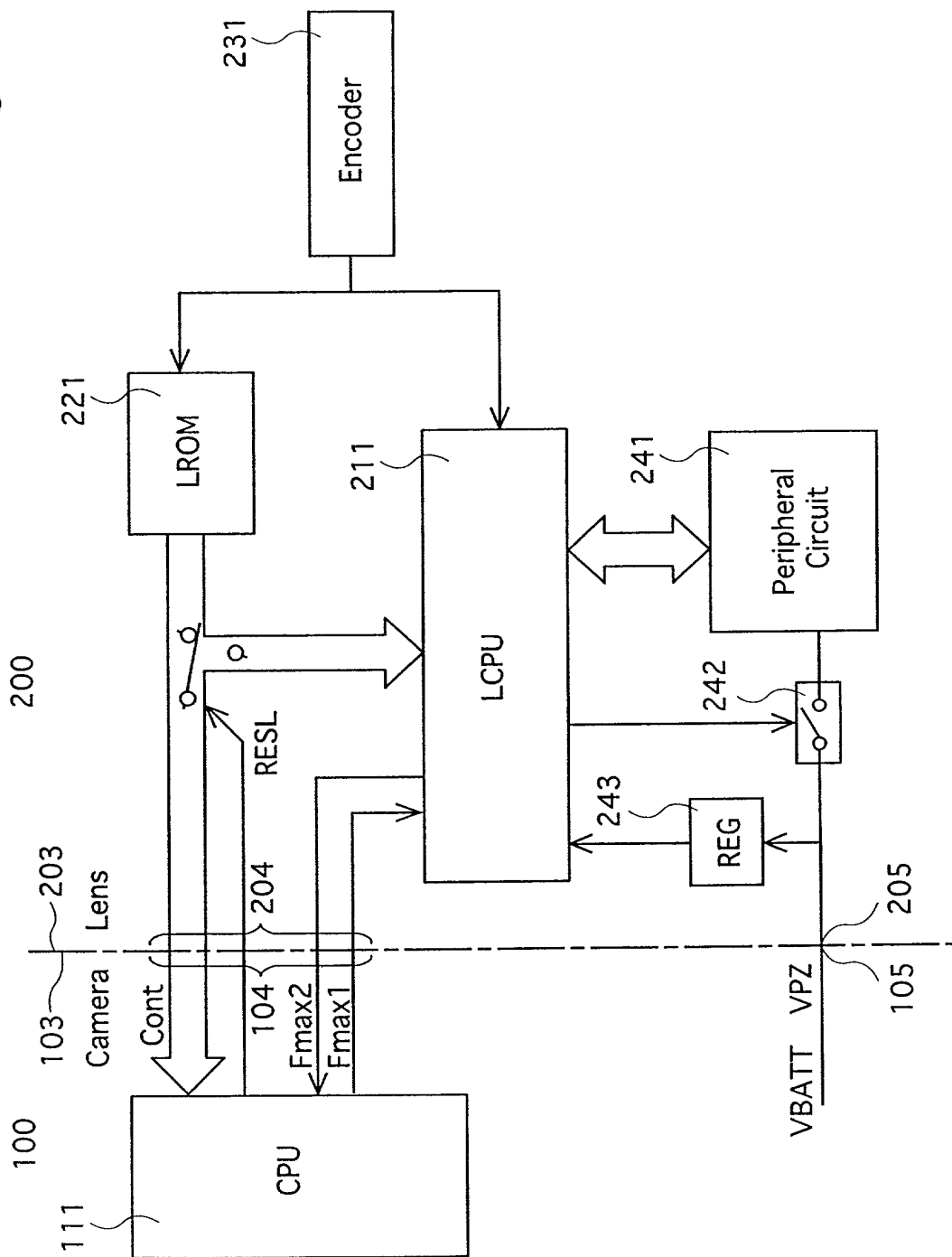


Fig. 2

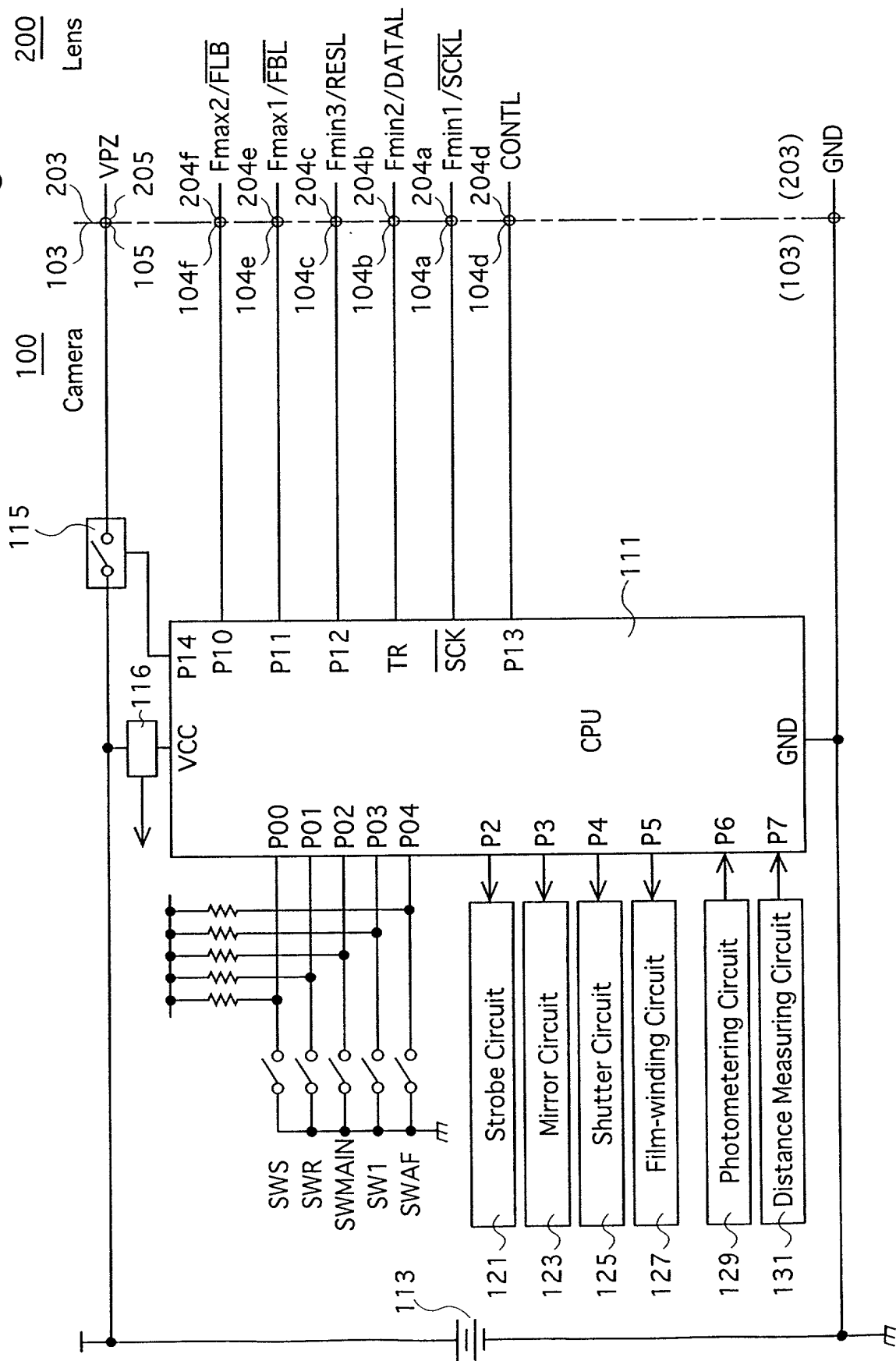


Fig.3

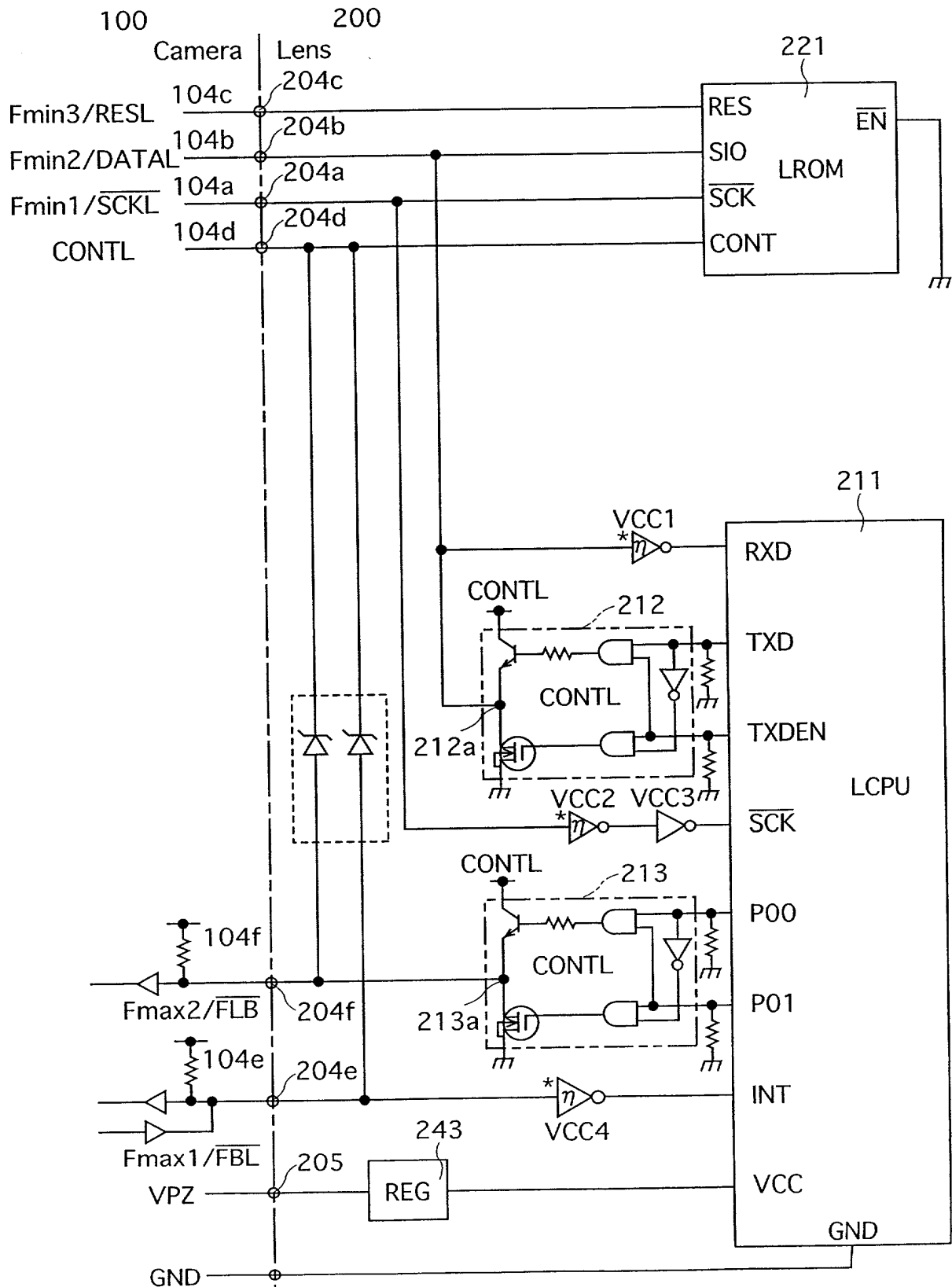


Fig.4

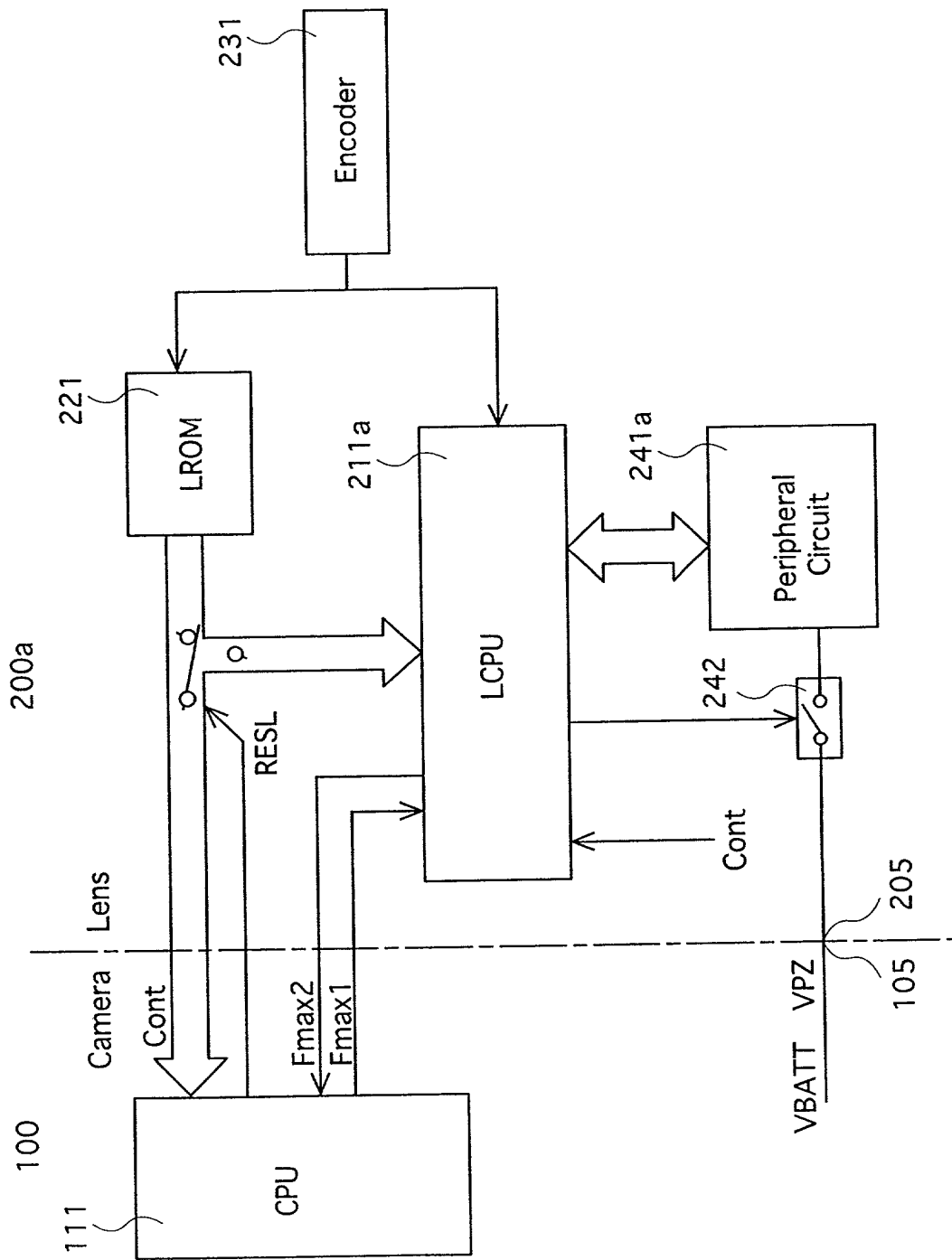


Fig. 5

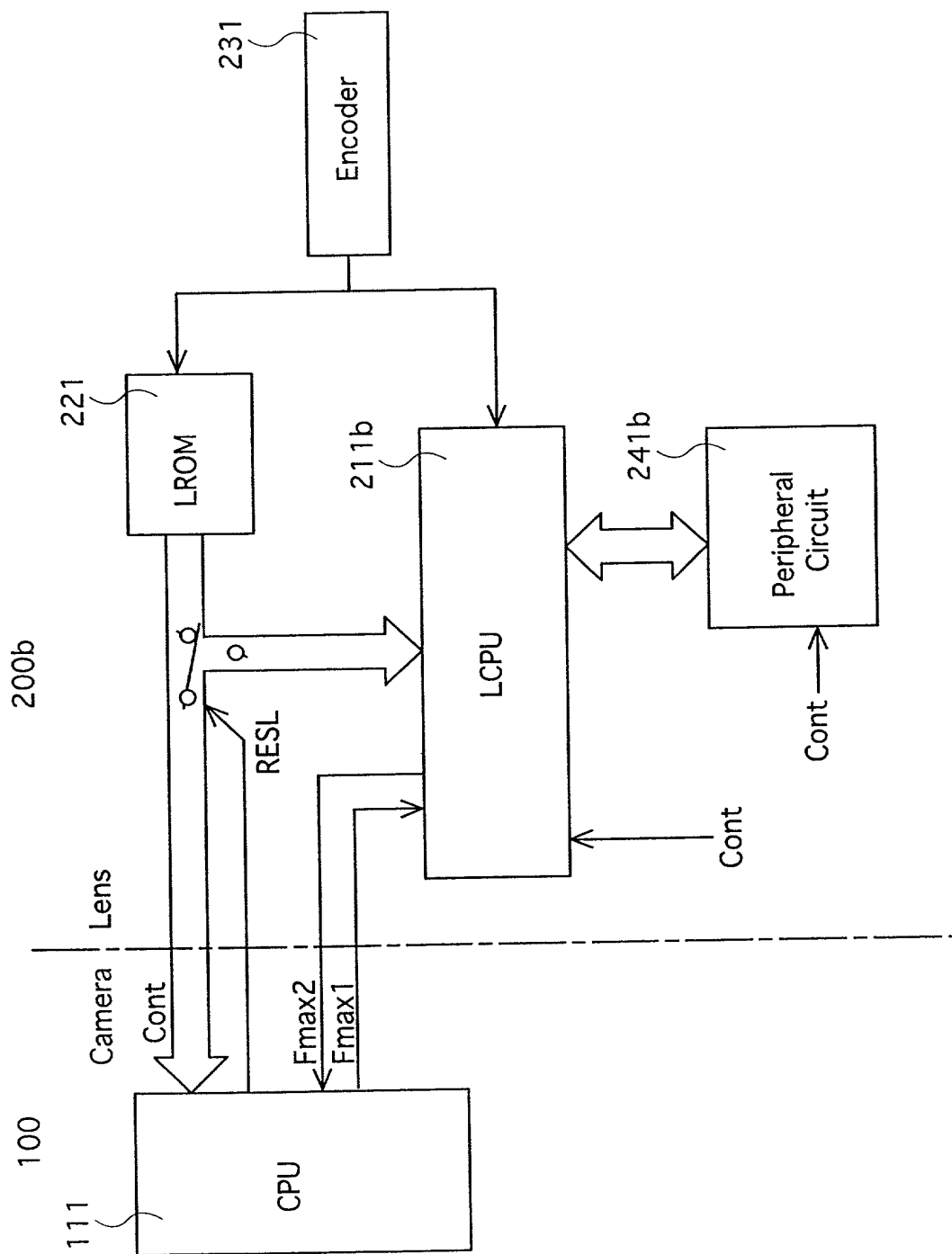


Fig. 6A

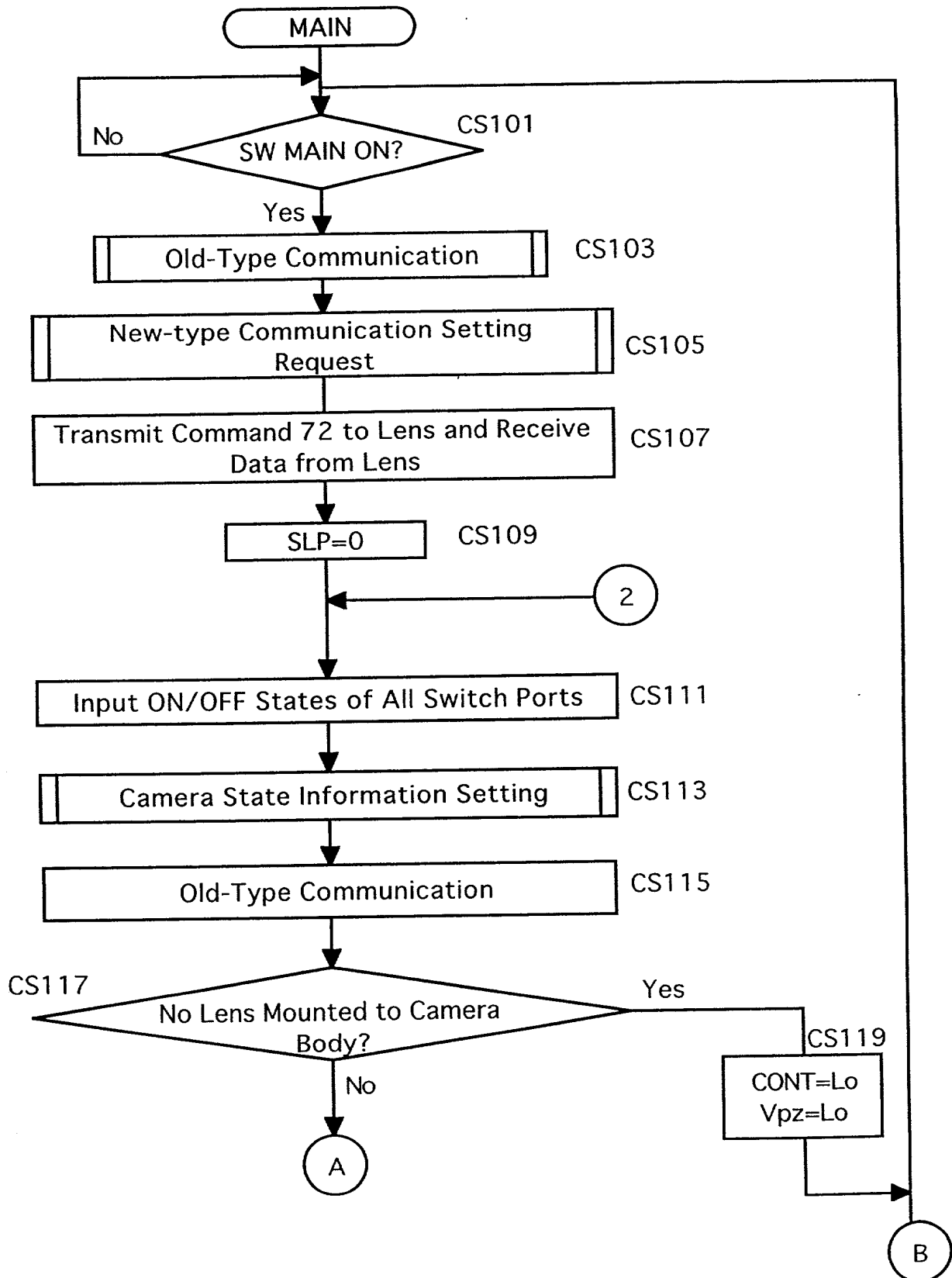


Fig. 6B

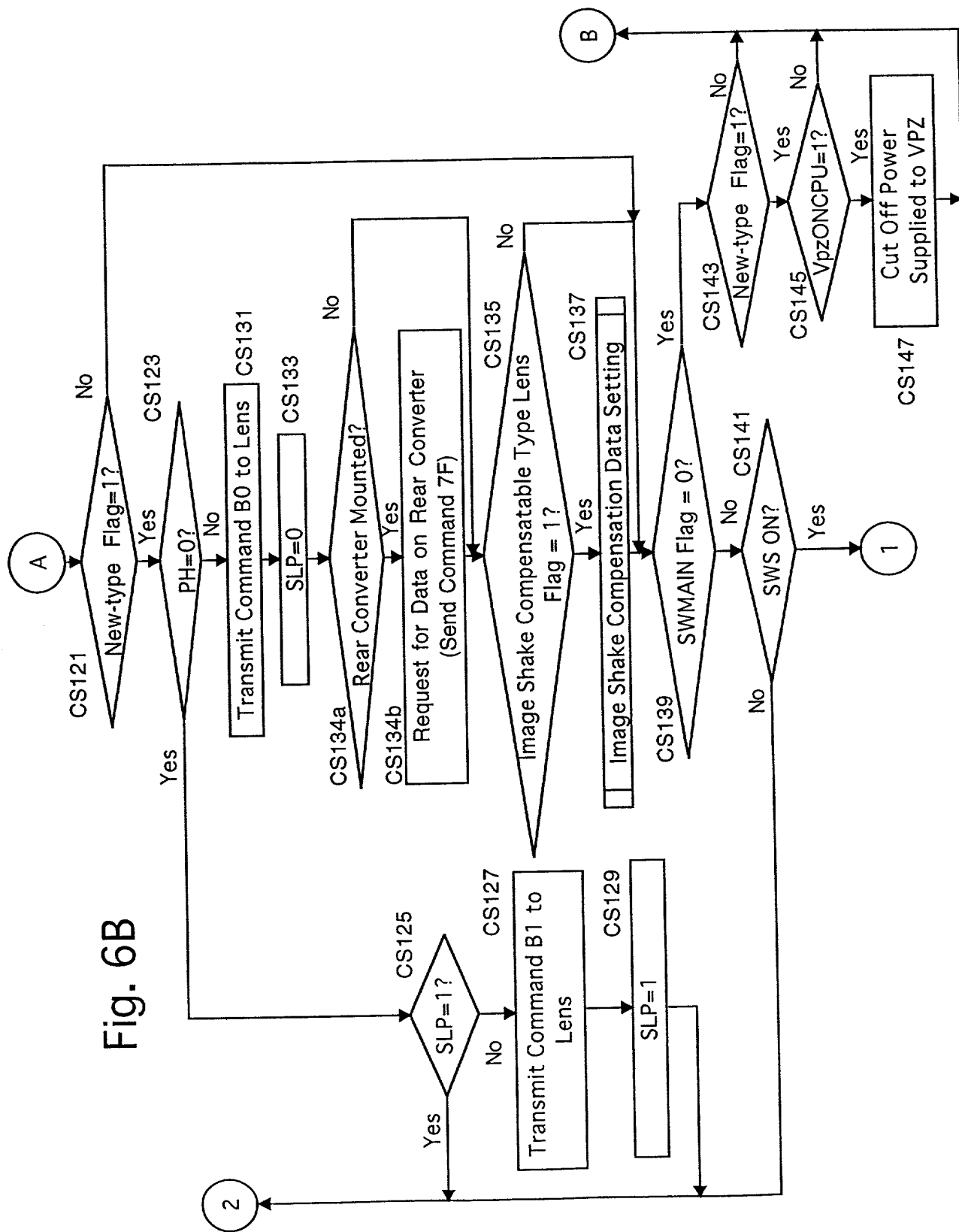


Fig. 7

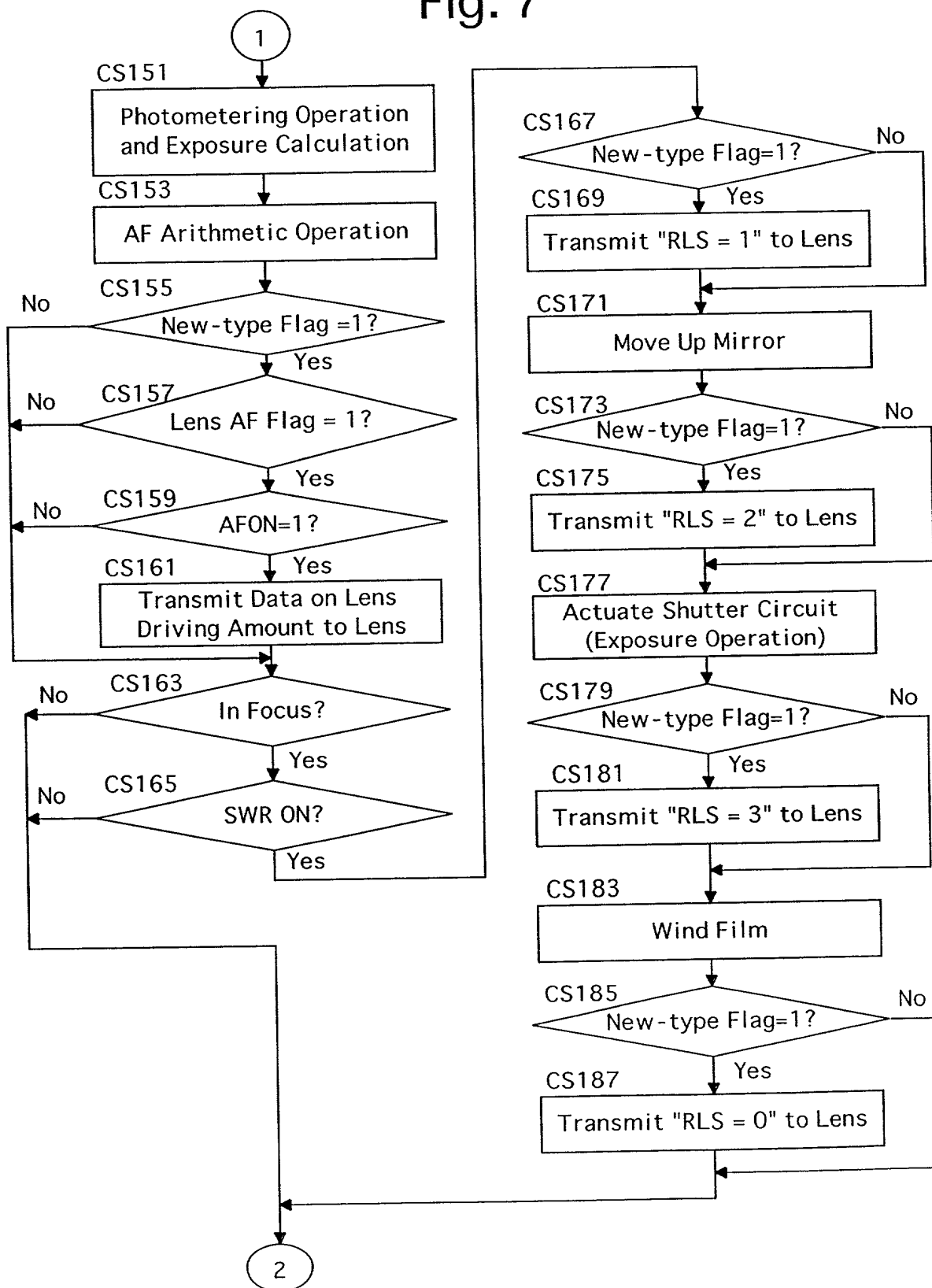


Fig. 8A

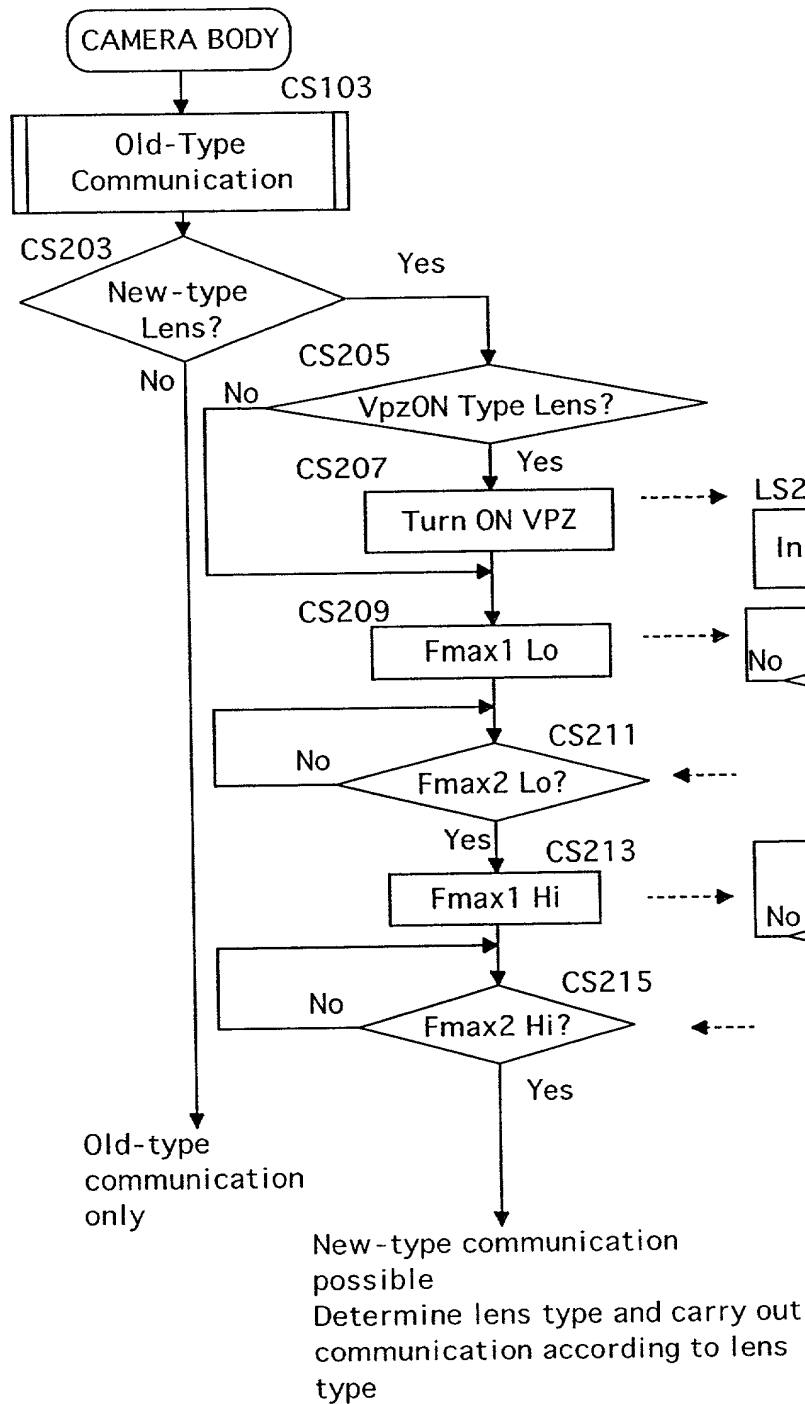


Fig.8B

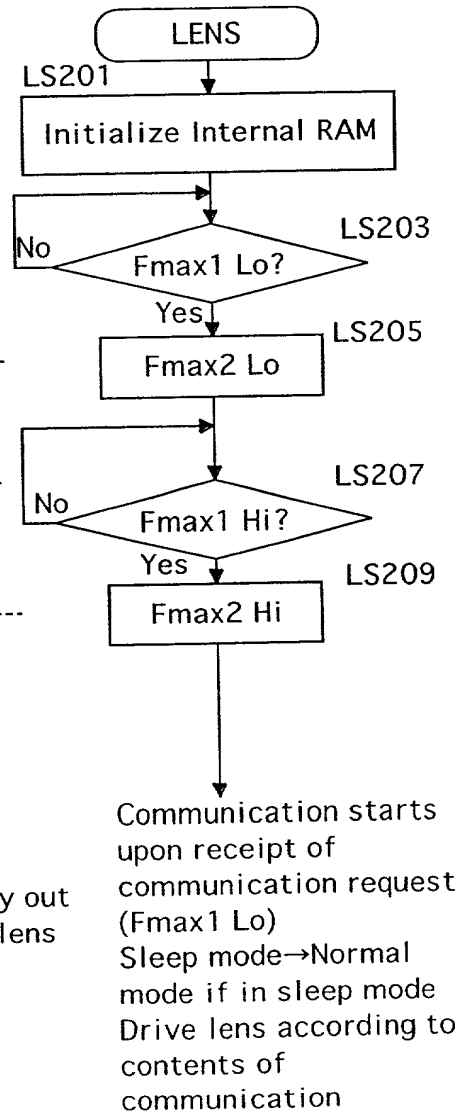


Fig.9

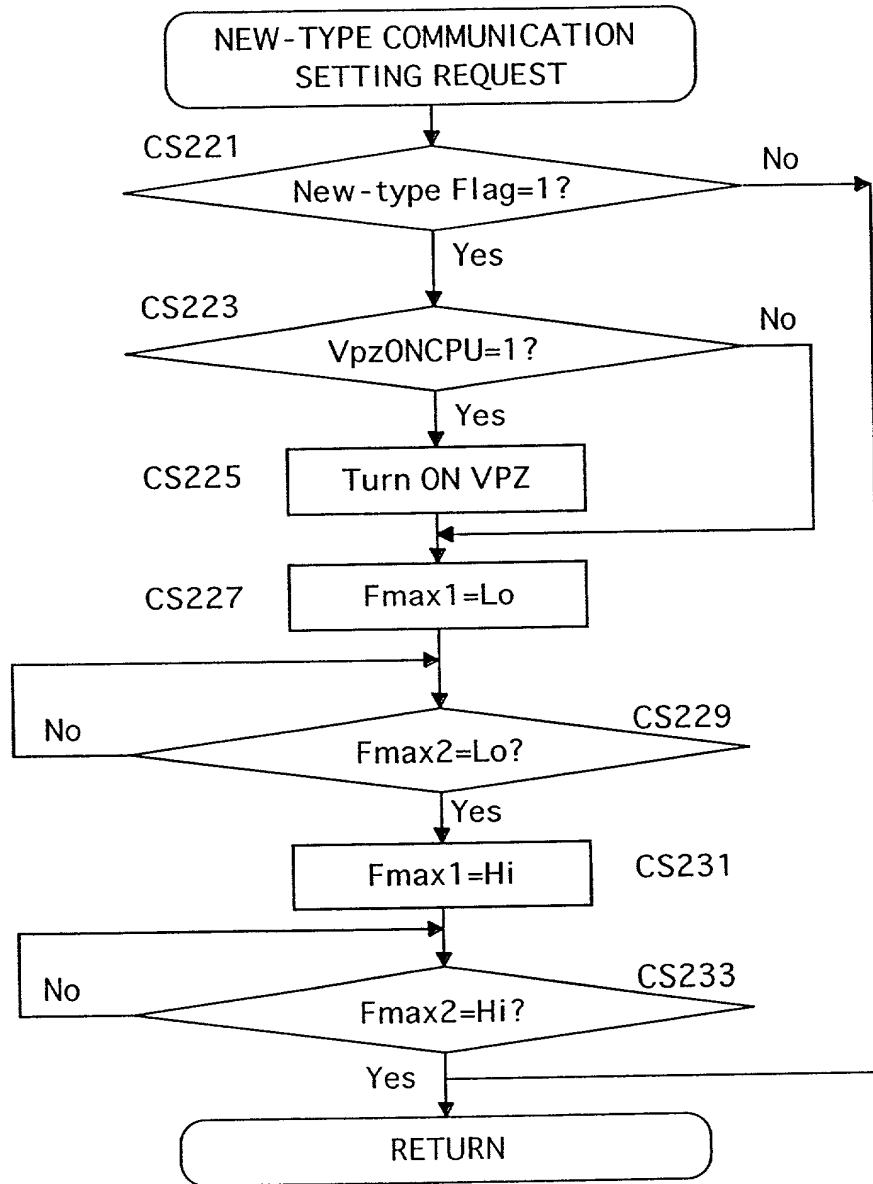


Fig.10

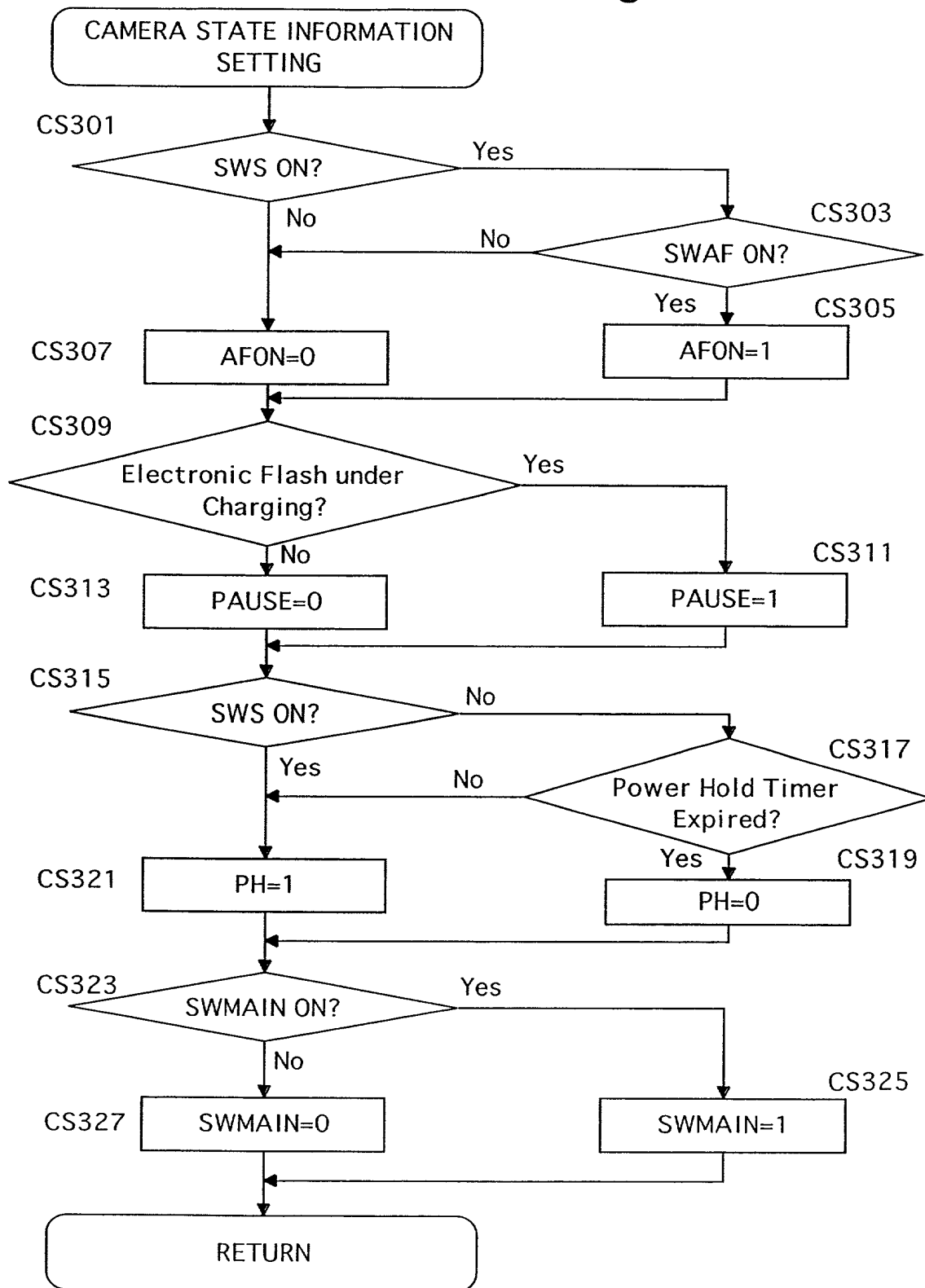
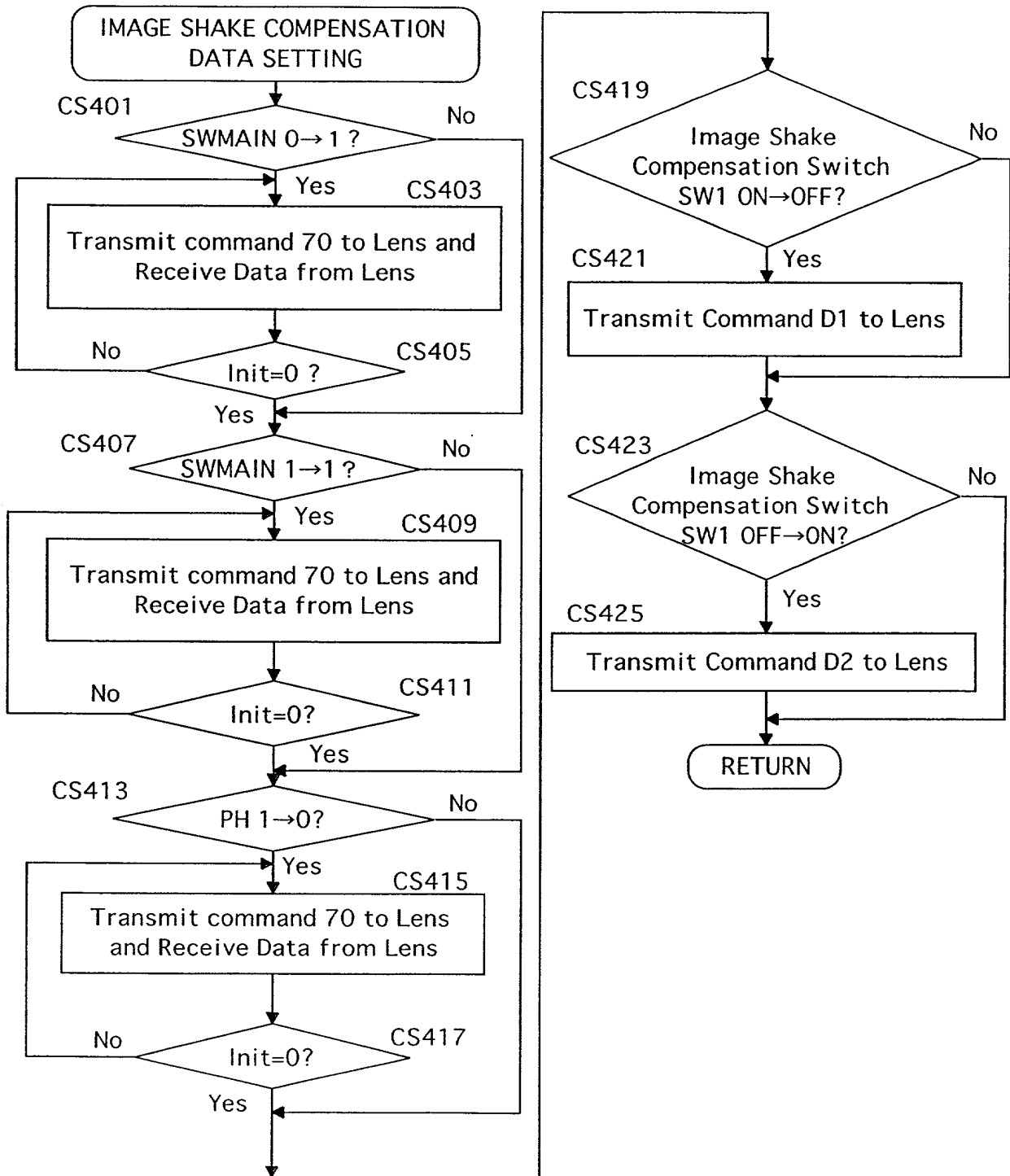


Fig.11



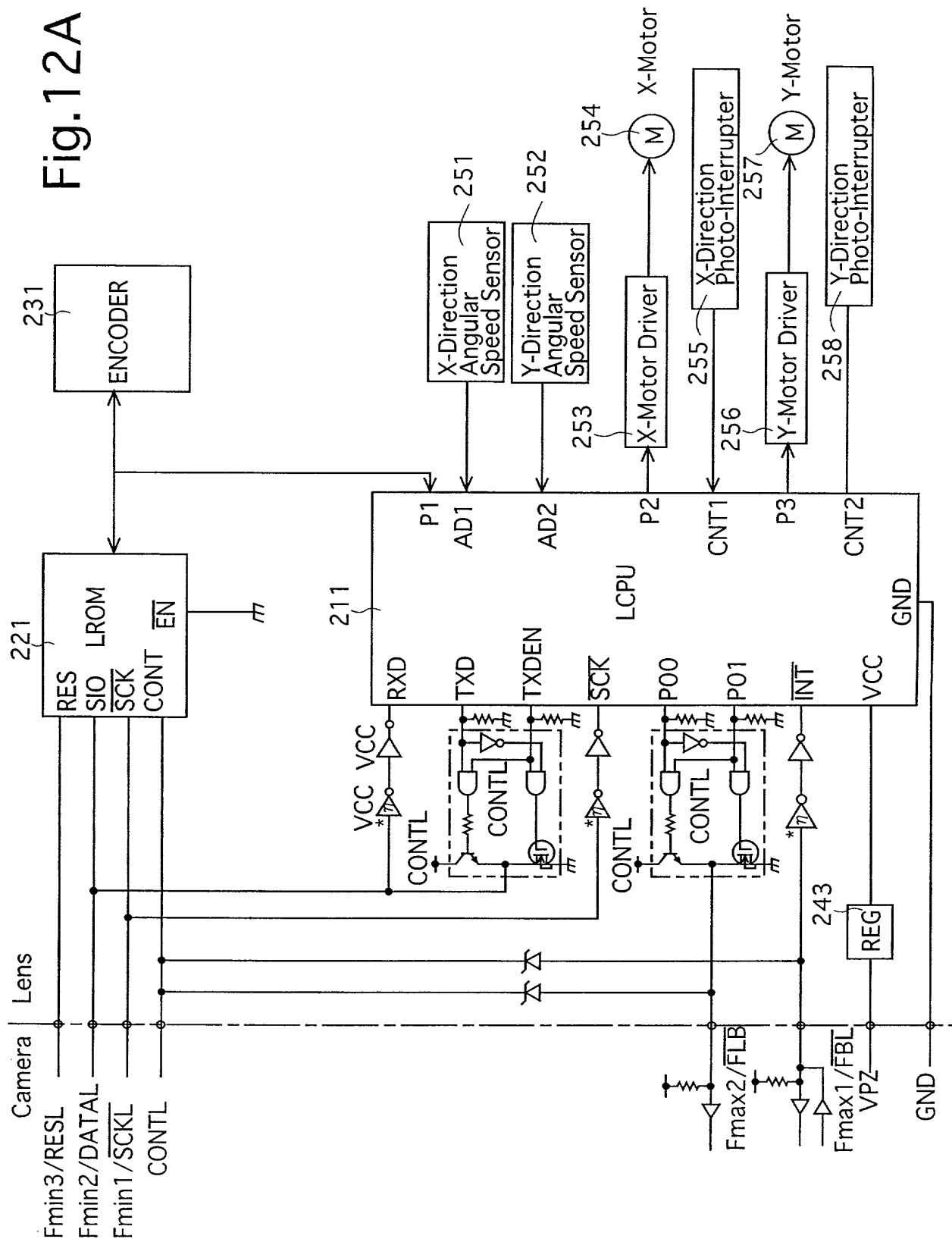


Fig. 12A

Fig. 12B

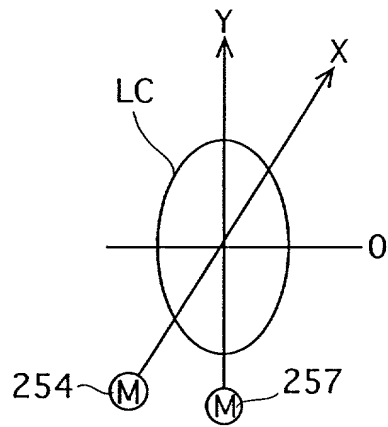


Fig.13

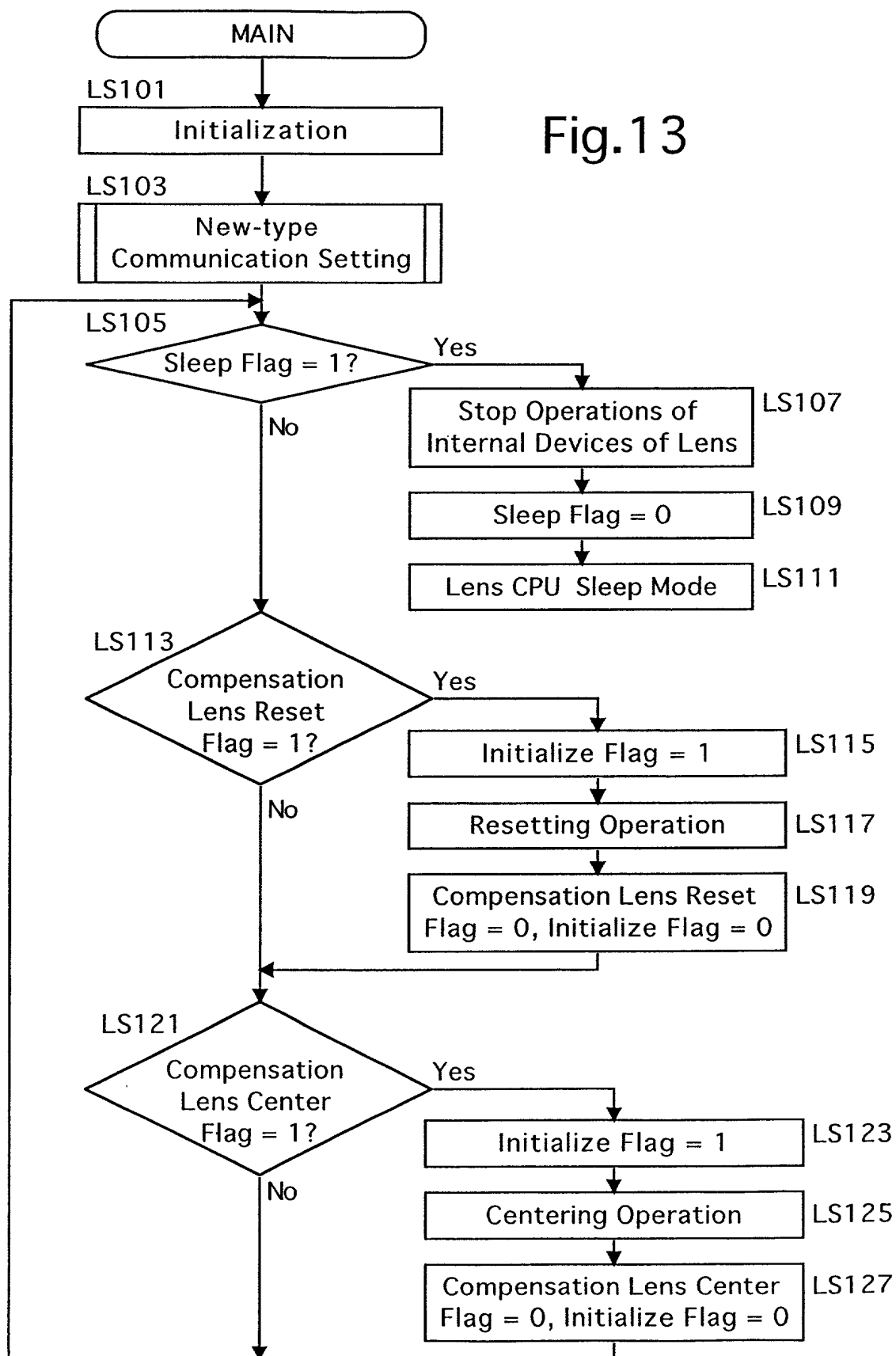


Fig.14

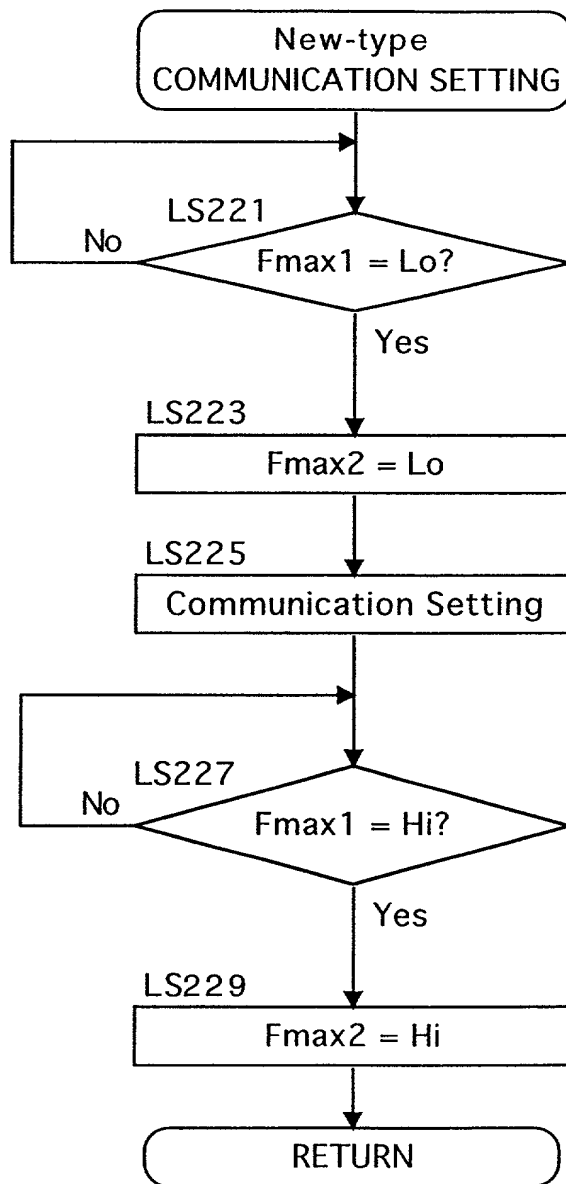
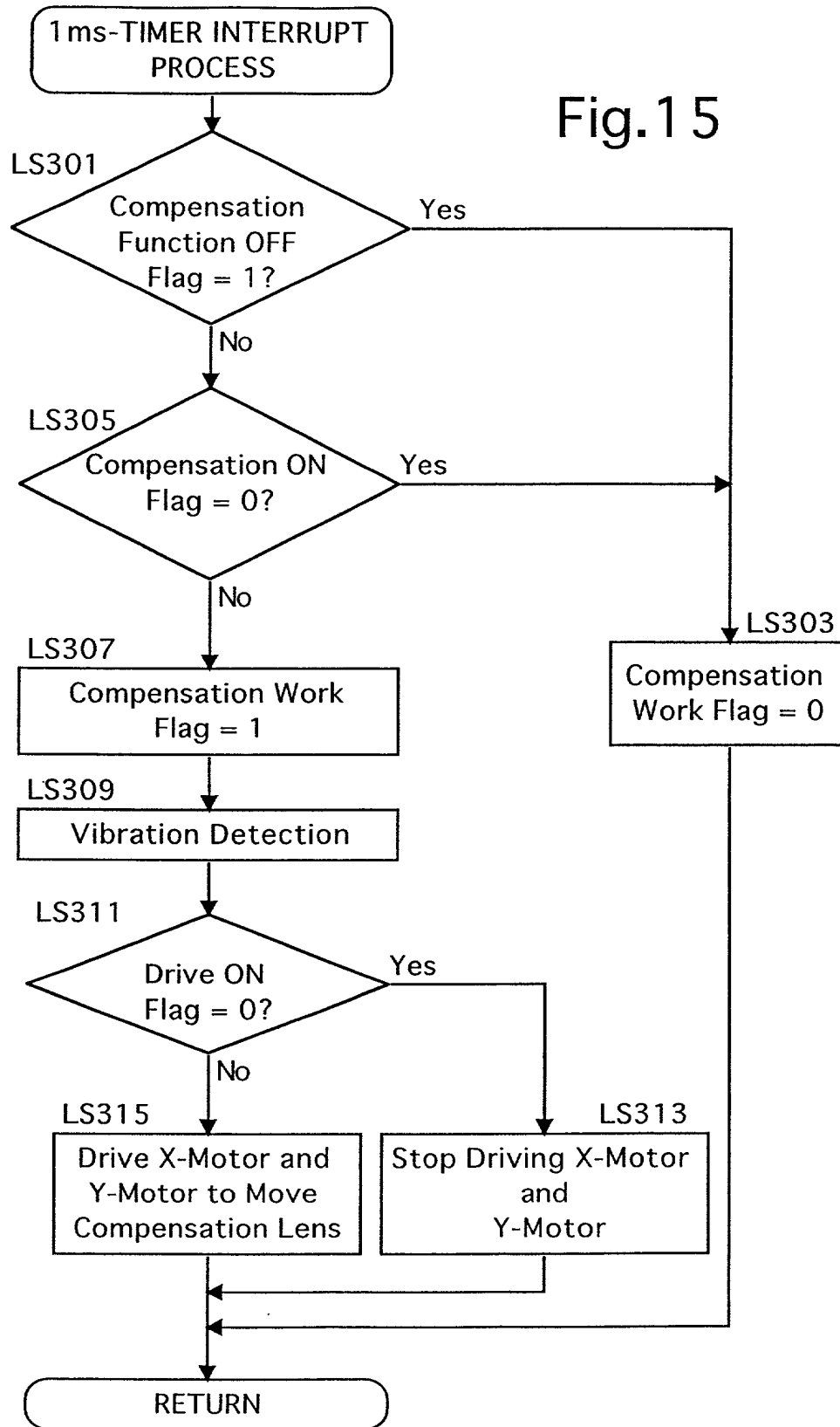


Fig.1 5



INVERSE-INT INTERRUPT PROCESS

Fig.16

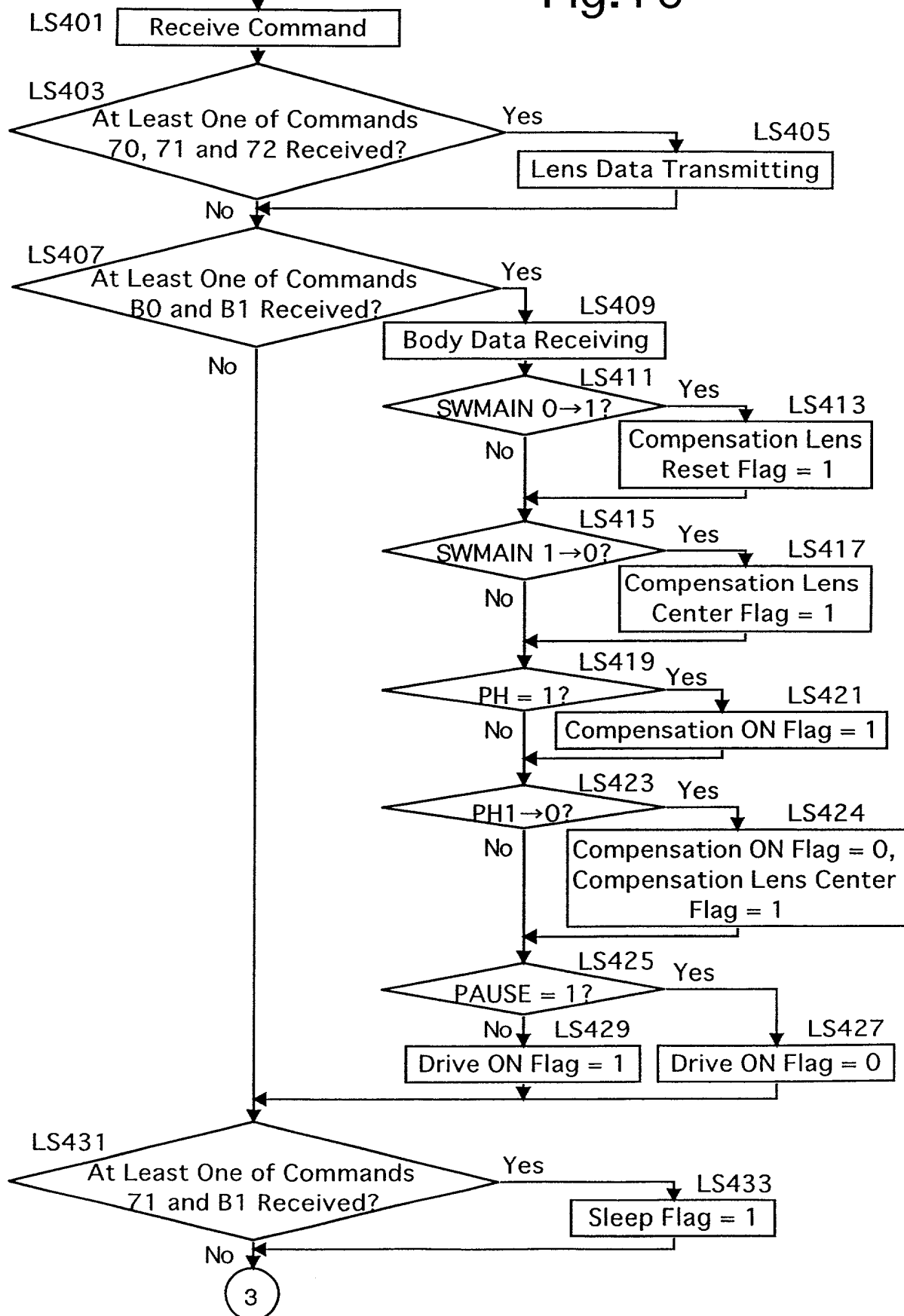


Fig.17

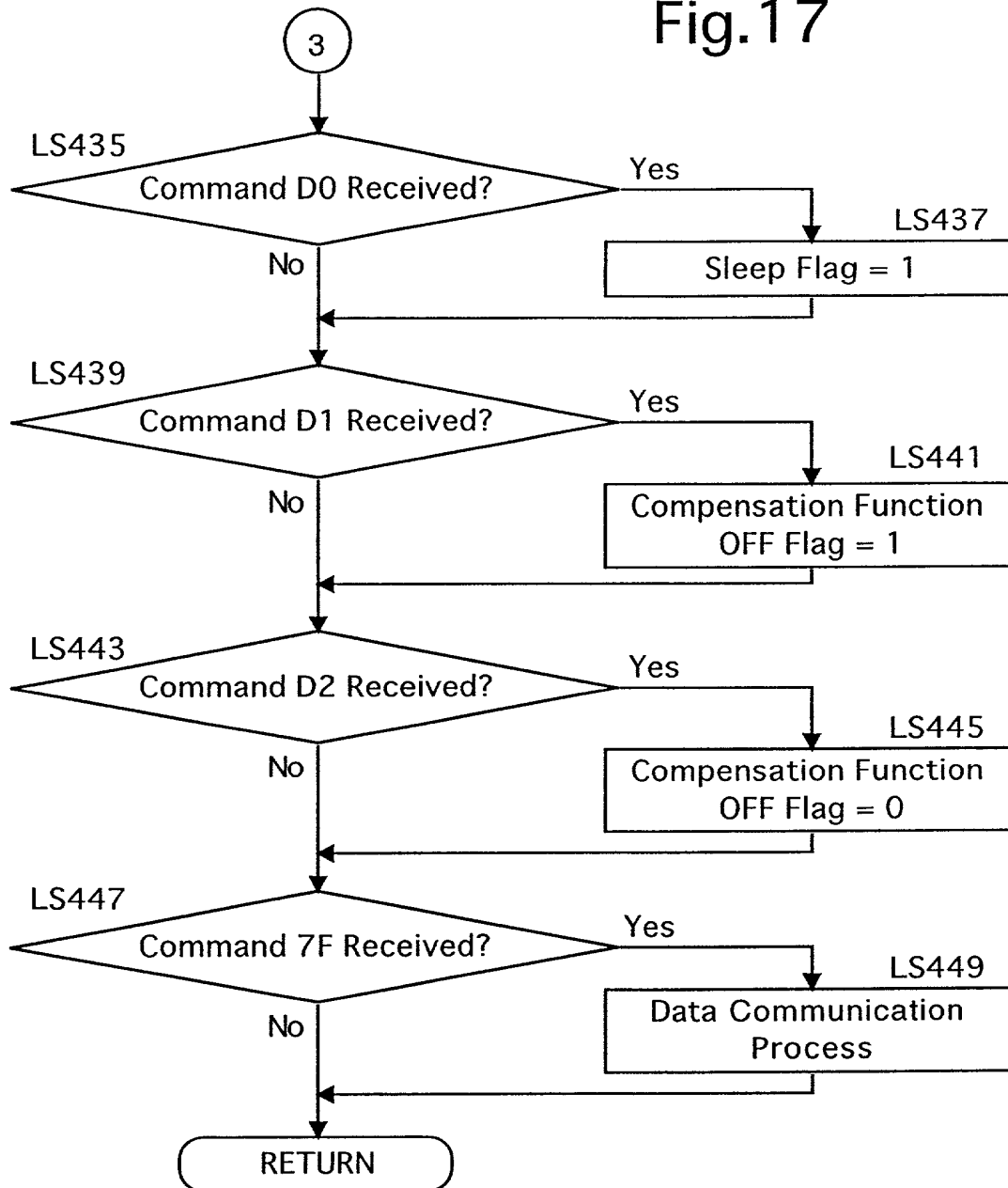


Fig. 18

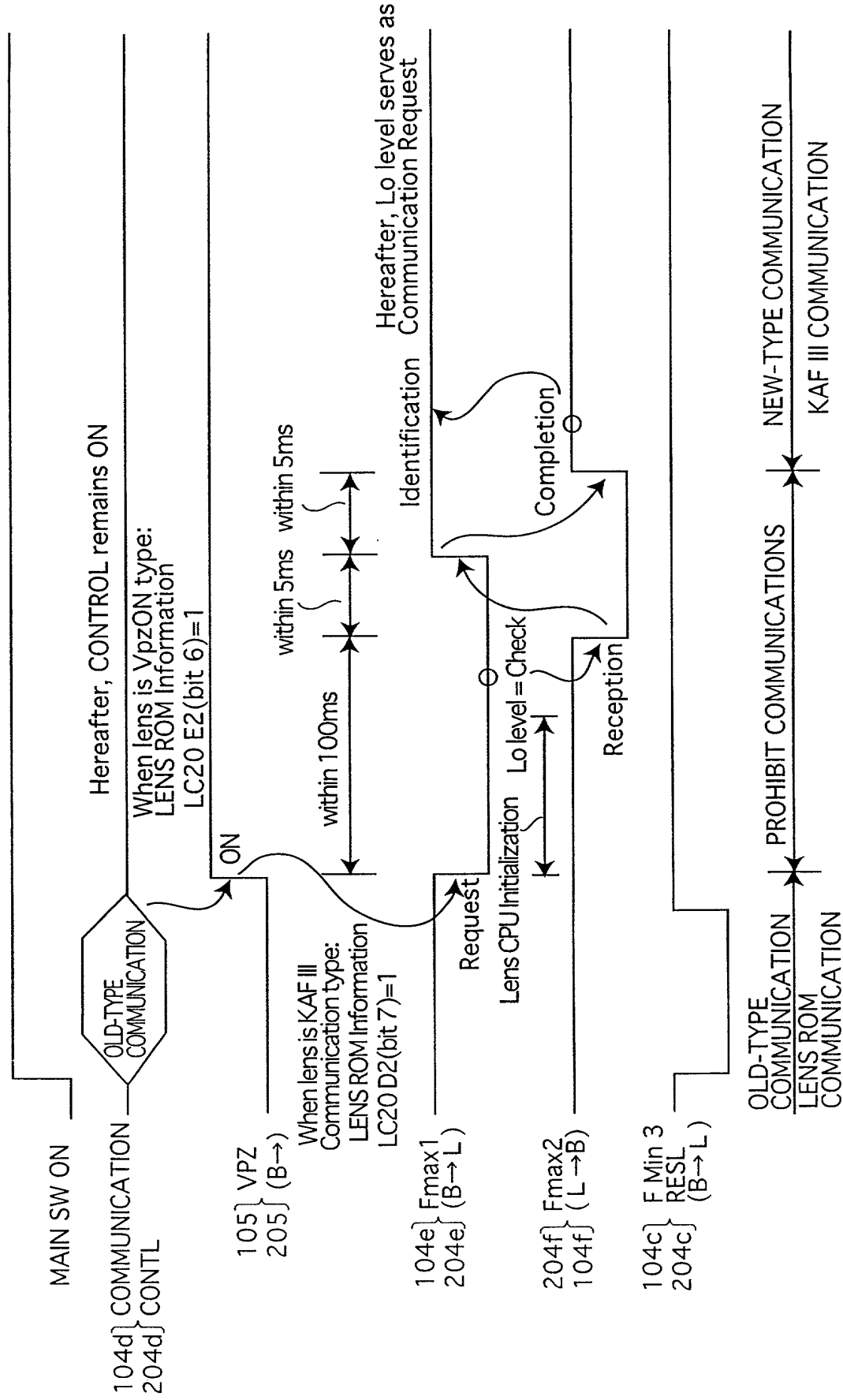


Fig. 20

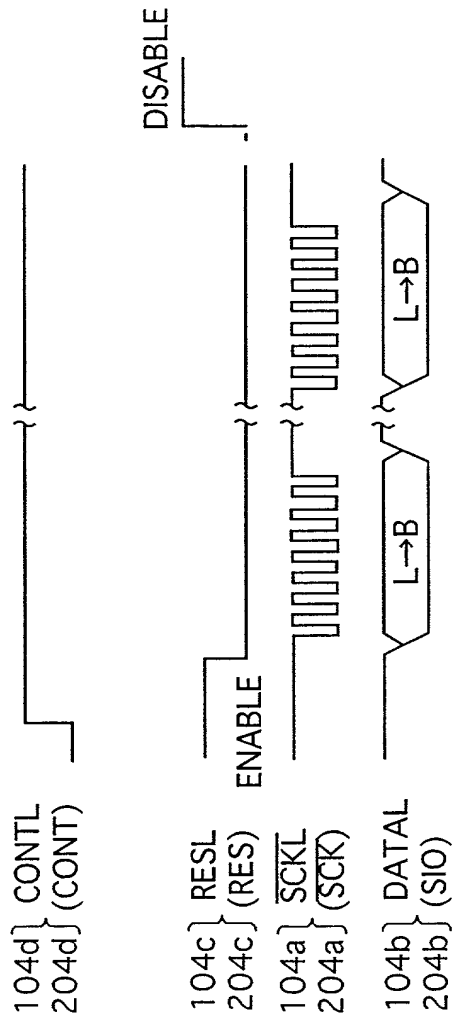
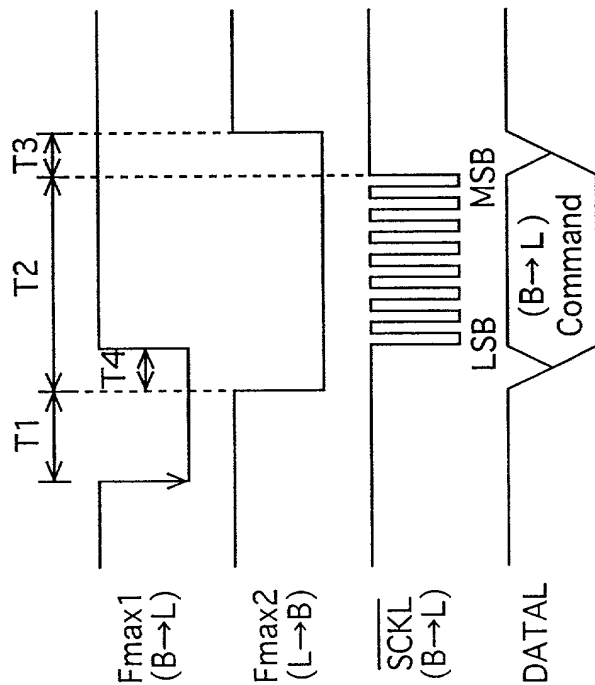
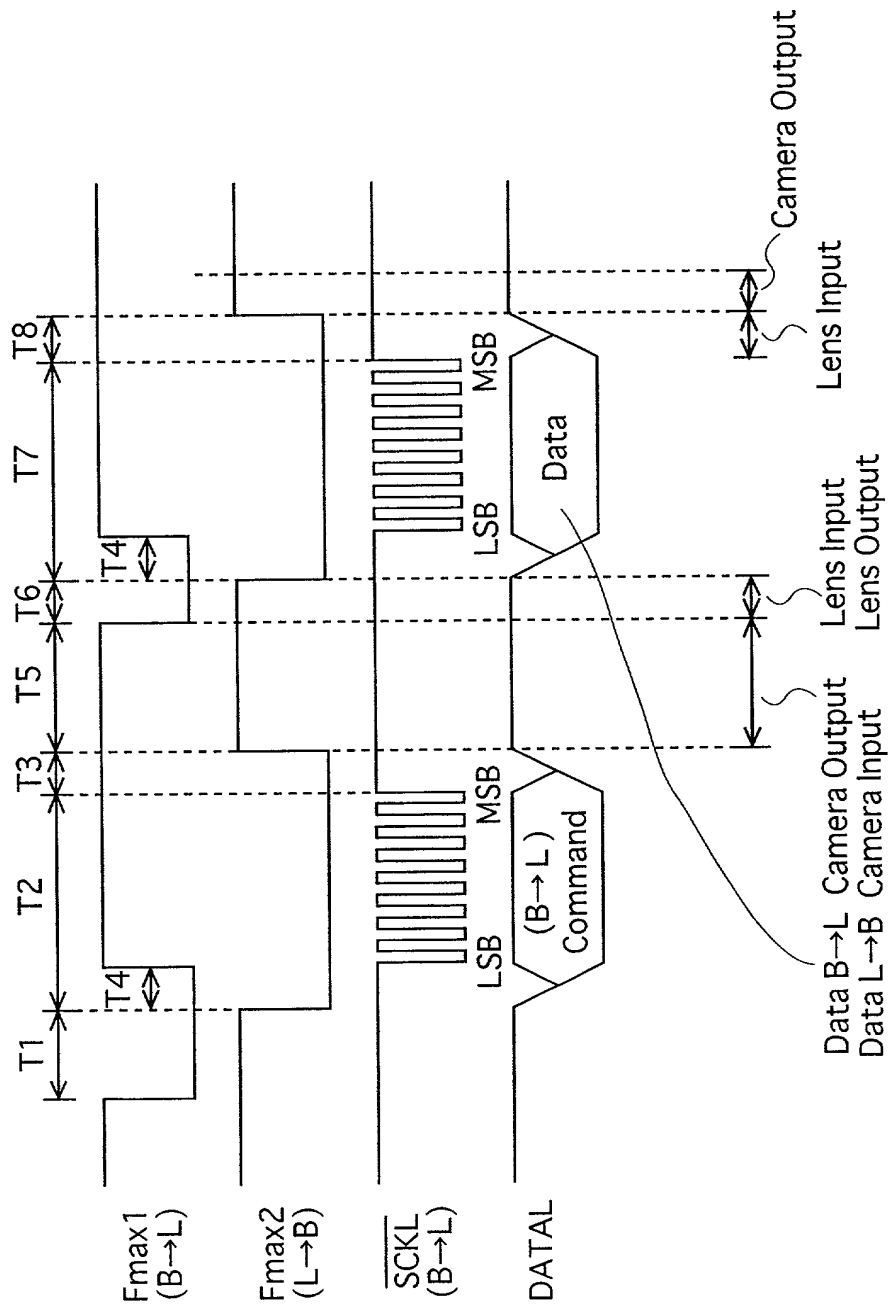


Fig.21A



- T1: within 50ms
- T2: within 5ms
- T3: within 5ms
- T4: within 5ms
- T5: within 5ms
- T6: within 5ms
- T7: within 5ms
- T8: within 5ms
- T9: within 5ms

Fig.21B



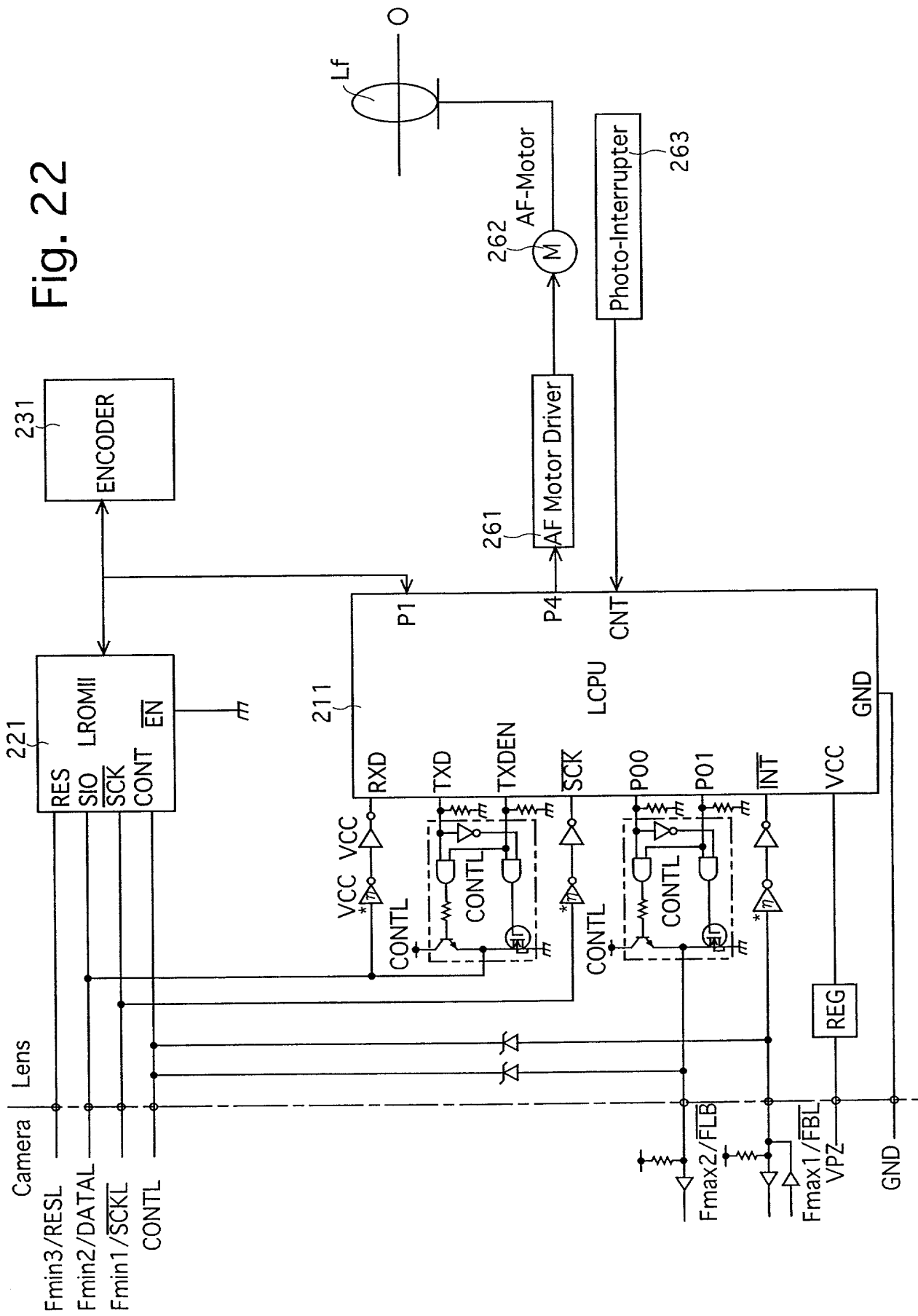


Fig. 23

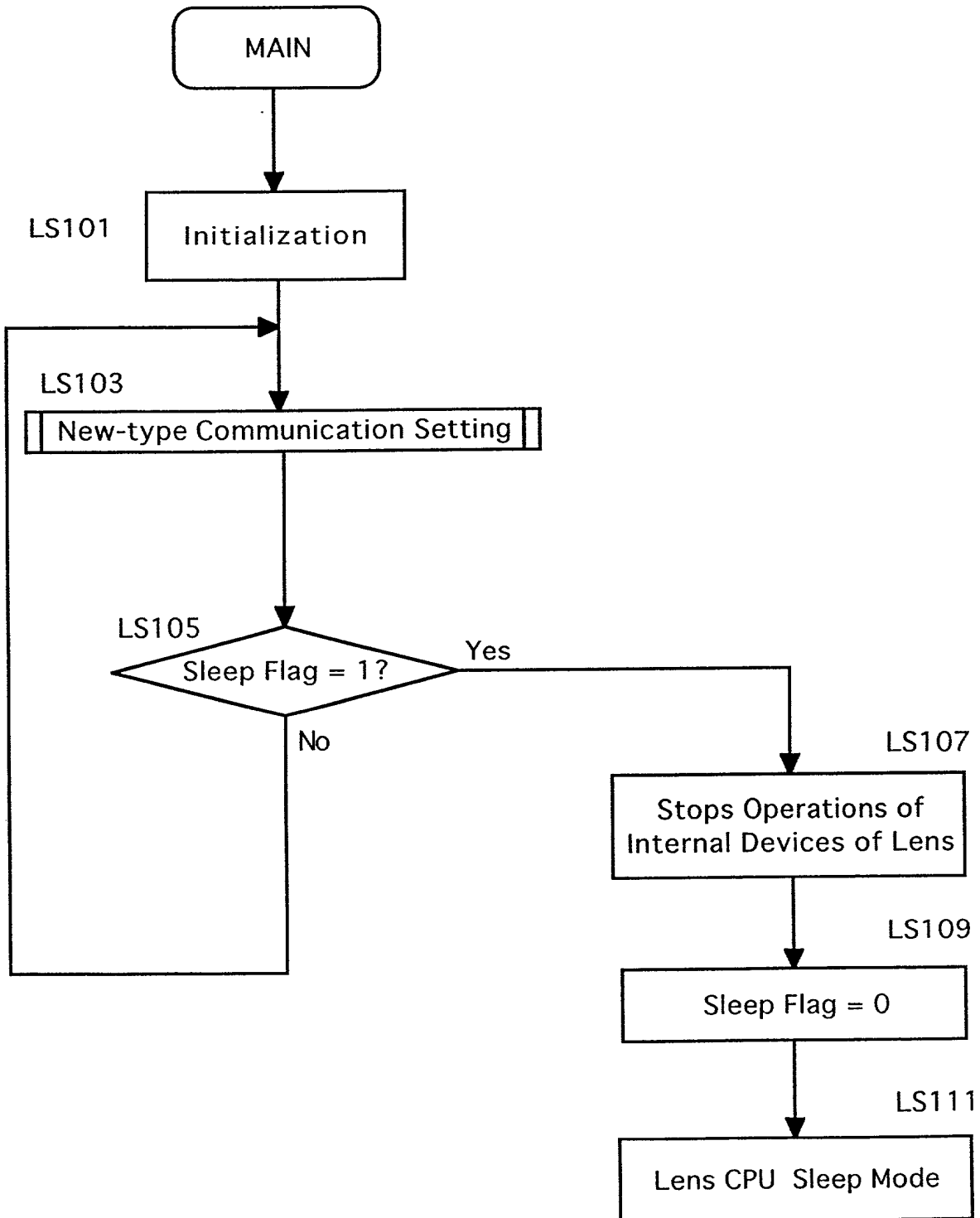
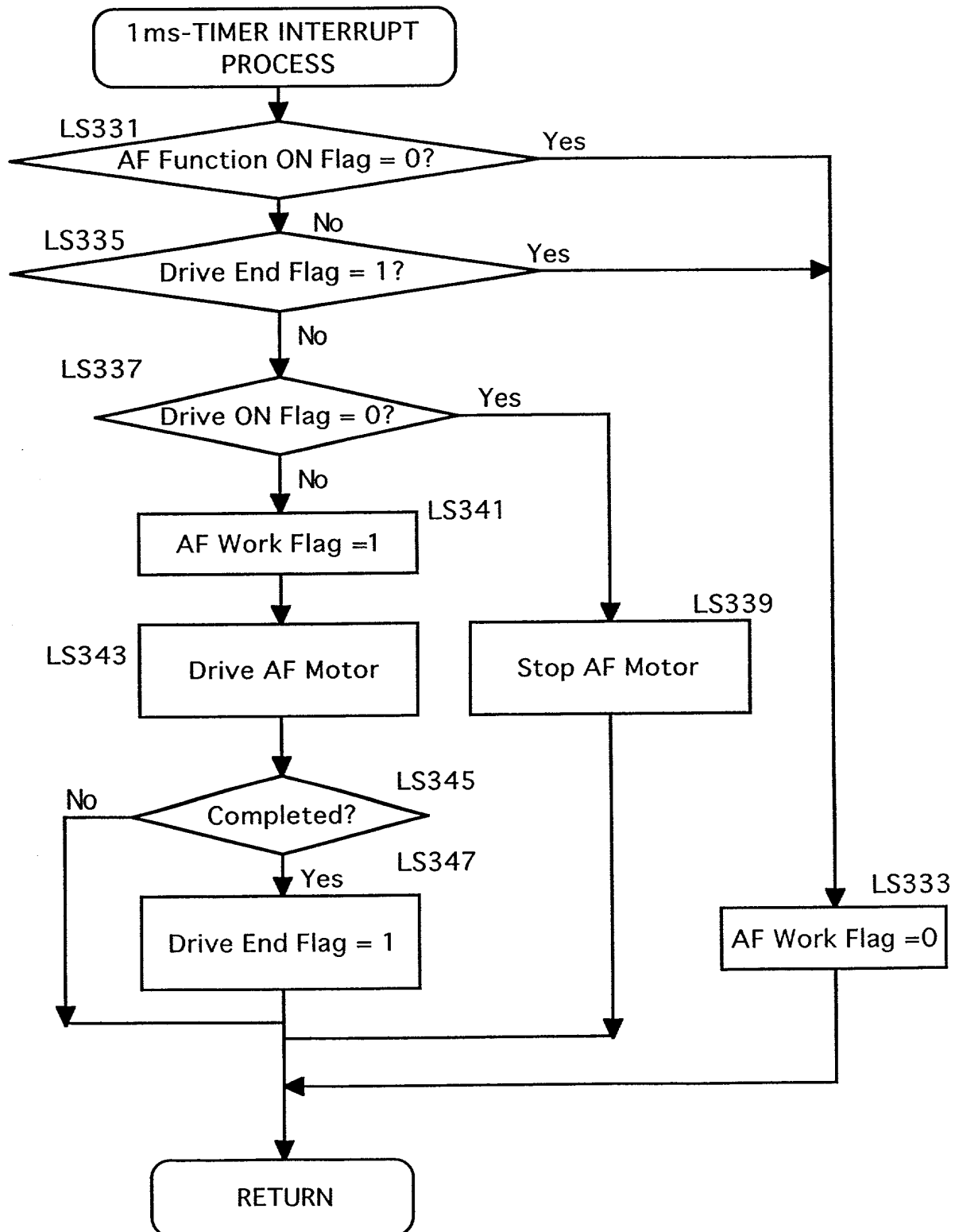


Fig. 24



INVERSE INT INTERRUPT PROCESS

Fig. 25

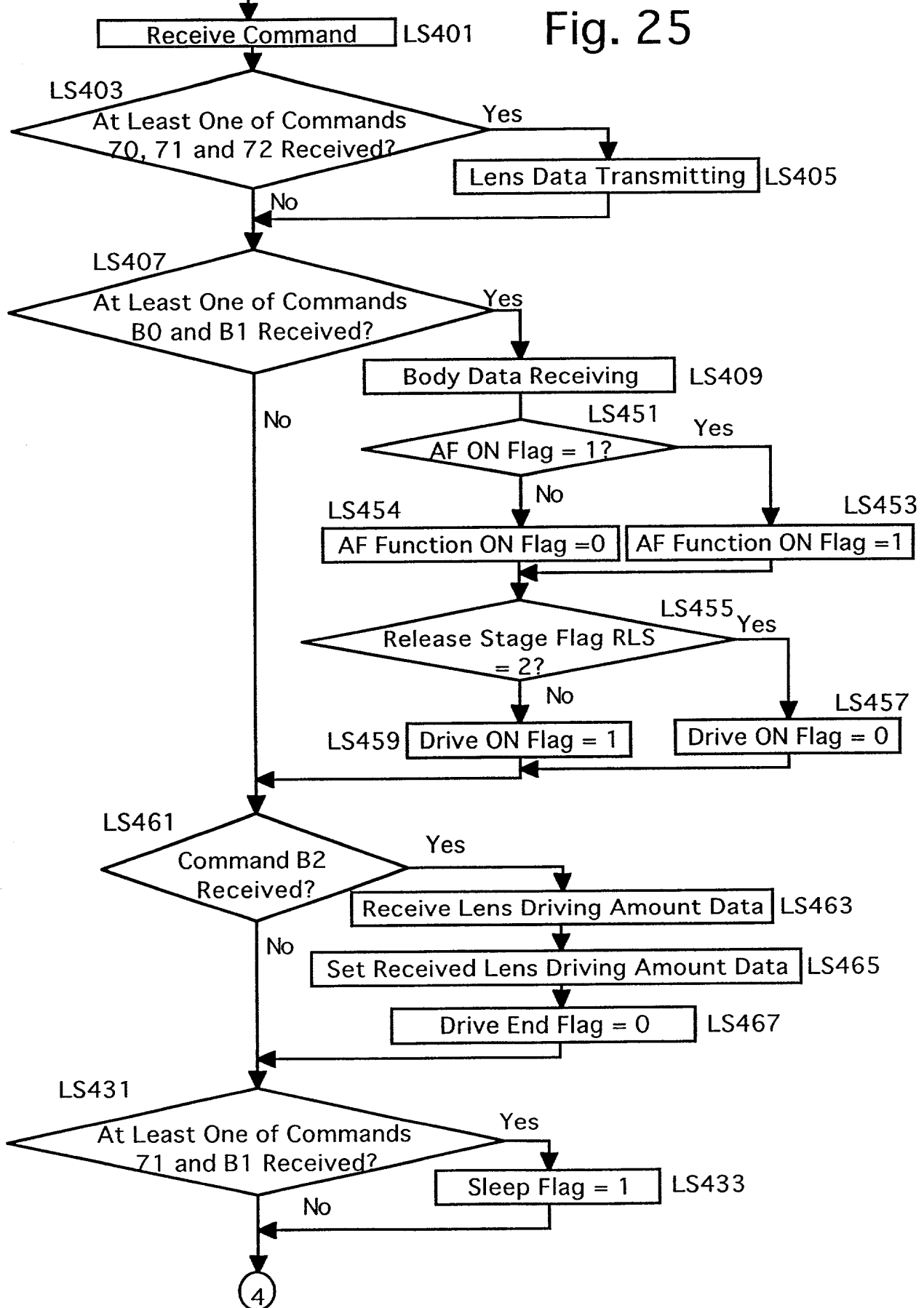


Fig. 26

